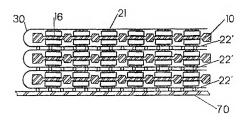
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(54) Title: HIGH-DENSITY, INTEGRATED CIRCUIT CHIP PACKAGE



(57) Abstract

A high-density package for integrated circuit chips (20) is provided. A plurality of integrated circuit chips (20) are mounted on opposite sides of a thermally conductive member (10) which serves as a stiffener for the package. A carrier member (30) is provided with a preselected, electrically conductive pattern, and is arranged to face a surface of each of the integrated circuit chips (20) and to be electrically thereto. This forms a compact package with heat dissipation properties.

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HIGH-DENSITY, INTEGRATED CIRCUIT CHIP PACKAGE

TECHNICAL FIELD

The present invention relates to a high-density package for integrated circuit chips. More particularly, the present invention relates to a high-density package for integrated circuit chips with thermal enhancement capabilities.

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BACKGROUND OF THE INVENTION

The field of computers has made substantial improvements throughout the years. Most of the improvements deal with increasing the memory capacity of the computers. At the same time, there is great effort in decreasing the size of the computers so that portable computers and notebook-sized computers presently have substantial memory capacity, easily equaling the capacity of desktop computers of just a few years ago.

The different types of memory generally include integrated circuit chips which are mounted on printed circuit boards or other types of carriers. The integrated circuit chips are made smaller and smaller in dimension, and yet carry more and more electronic elements thereon. As the number of integrated circuit chips on a carrier increases, the heat generated by such chips poses a

substantial problem. Clearly, excessive heat will adversely affect the operation of the integrated circuits.

Therefore, the drive for increased memory capacity leads to more integrated circuits in smaller and smaller areas. This poses substantial problems to designers of high-density packages for integrated circuit chips.

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SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a high-density package for integrated circuit chips.

Another object of the present invention is to provide a highdensity package which has substantially improved thermal capabilities.

A feature of the present invention is to use a thermally conductive stiffener for mounting the integrated circuit chips thereon.

Still another feature of the present invention is to mount the integrated circuit chips on opposite surfaces of the thermally conductive stiffener, so as to increase the number of integrated circuit chips that may be mounted in a specific volume of the high-density package.

Still another feature of the present invention is to attach the integrated circuits mounted on the thermally conductive stiffener to a carrier member which can make electrical contact with the integrated circuit chips mounted on both sides of the thermally conductive stiffener.

Still, a further object of the present invention is to provide a high-density package which may be stacked with other similar high-density packages and mounted on a mother board for use as memory in a computer, for example.

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BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, and advantages of the present invention will become apparent upon further consideration of the following detailed description of the invention, when read in conjunction with the figures in which:

Figure 1 is a top view of a thermally conductive stiffener used for mounting integrated circuit chips in accordance with the first embodiment of the present invention;

Figure 2 is a top view of a stiffener used for mounting a plurality of columns of integrated circuit chips in accordance with the present invention;

Figure 3 is a side view, partially in section, of a high-density package constructed in accordance with an embodiment of the present invention.

showing the thermally conductive stiffener, the integrated circuit chips, and a carrier;

Figure 4 is a side view, partially in section, of an embodiment similar to that of Figure 3, with a different type of carrier;

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Figure 5 is a side view, partially in section, of another embodiment of the stiffener with cooling passages of the high-density package; and

Figure 6 is a side view, partially in section, of a high-density package including a plurality of stacked packages.

DESCRIPTION OF THE INVENTION

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Referring to the drawings, and more particularly to Figure 1, it can be seen that a thermally conductive stiffener 10 is provided with a plurality of areas 12 adapted to mount an integrated circuit package thereon. The thermally conductive stiffener is shown in the side view in Figure 3, with integrated circuit chips 20 mounted thereon.

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It can be seen that the thermally conductive member 10 has a pair of opposite sides 11 and 13. In Figure 3, 11 is the bottom side, whereas 13 is the upper side.

The integrated circuit chips 20 are shown mounted in the preformed areas 12 on both sides of the member 10. Thus, a plurality of integrated circuit chips are shown mounted in Figure 3, such chips being mounted on the pair of opposite sides of the member 10.

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The integrated circuit chips 20 may be mounted in the areas 12 by using a high-thermal conductivity paste 16 arranged between one of the surfaces of the integrated circuit chips 20 and the member 10. The other surface of each of the integrated circuit chips are connected, in Figure 3, to a flexible carrier 30.

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The carrier 30 is bent around the member 10 so that it faces both sides of the member 10. The carrier 30 will have an electrically conductive pattern formed thereon, adapted to connect to the integrated circuit chips 20. The carrier 30 is connected to the other surfaces of the integrated circuit chips 20 by means of solder bumps 21 in a conventional manner such as controlled-collapse-chip-connection (C4), wire bond, or thermocompression bond arrangement.

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As noted above, the carrier 30 in Figure 3 is a flexible carrier so that the arrangement shown in Figure 3 makes connections to all of the

integrated circuit chips 20 mounted on the member 10 utilizing a very small volume. The carrier 30 may be connected to other carriers or a mother board by the use of solder balls 22, shown connected to the bottom of the carrier in Figure 3.

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While only a side view of the member 10 is shown in Figure 3, it can be seen that the member 10 can have a single strip of integrated circuit mounting areas 12 or, as shown in Figure 2, a member 10' can have a plurality of columns of mounting areas 12' for mounting integrated circuit chips, depending on the memory and capacity required.

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Similarly, the member 10 is made of a high thermally conductive material, such as aluminum, copper, or Thermalgraph 8000^{rm} (trademark). The member 10 in Figure 3 not only serves to provide heat dissipation, it also serves as a stiffener, so that the high-density package shown in Figure 3 is very compact and yet provides a stable arrangement for mounting the integrated circuit chips and providing interconnections thereto. Because the stiffener is made of a thermally conductive material and a high thermal conductivity paste is used for attaching one surface of the integrated circuit chips to the stiffener, heat generated by the operation of the integrated circuit chips is quickly

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dissipated into the air circulating about the stiffening member 10. The stiffening member 10 may also have fins, extensions or heat pipes attached if desired.

The solder balls 22 may be used to attach the carrier 30 to a second level, as will be explained subsequently.

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Referring now to Figure 4, a different type of carrier is shown. Here the carrier is formed in two parts 40 and 50. The carrier can be a printed circuit board made of FR4 material which is a metallic or copper plane arranged with the appropriate electrical circuit pattern thereon or from other packaging material such as teflon or ceramic. The electrical connections between the parts 40 and 50 of the carrier in Figure 4 are made by an integral, flexible cable 41. The parts of Figure 4 that are the same as the parts of Figure 3 are similarly numbered since the remaining elements of the high-density package, aside from the carrier, remain the same.

Because the two-part carrier 40 and 50 face the opposite surfaces of the integrated circuit chips, and the stiffener 10 is made of thermally conductive material, heat is readily dissipated from the integrated circuit chips into the environment, even though the high-density package is unusually compact.

The embodiment of Figure 5 shows a different type of stiffener member 60. The member 60 is formed with a plurality of channels 61 therethrough in the form of a "cinder block" arrangement. The channels 61 may have any desirable cross section depending on the application. In this arrangement, increased heat dissipation surfaces are provided by the stiffener 60. In the embodiment of Figure 5, the elements numbered similarly to that of Figures 3 and 4 serve similar functions.

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With the channels 61, a higher degree of heat dissipation may be provided when necessary. It is seen, however, that the member 60 contains mounting areas 12 for the circuit chips 20, as before. Also, in this figure, a flexible carrier 30 is used for facing the opposite sides of the stiffener 60 and the other surfaces of the integrated circuit chips 20.

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Referring to Figure 6, an arrangement is shown in which three carriers 30 are provided to form a multi-stack or multi-level arrangement. Each of the carriers contains a package of the type shown in Figures 3 or 5. This arrangement of Figure 6 forms a plurality of high-density packages for the

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integrated circuit chips. It can be seen that each carrier is electrically connected to the carrier adjacent thereto, and the last or bottom carrier in Figure 6 is connected to a mother board 70 by means of the solder balls 22'. Similar solder balls or solder bumps are used for connecting the carriers to the adjacent carriers. Wire bonds may also be used for this purpose.

Thus, a stacked, high-density package for integrated circuit chips is provided and provides an unusually compact arrangement having very good thermal conductivity. Each of the three packages shown in Figure 6 has a thermally conductive stiffener member which is able to dissipate quickly the heat generated by the integrated circuit chips to the surrounding environment. This will permit higher memory capacity to be provided in a smaller volume than previously permitted. Also, since the integrated circuit chips are mounted on both, opposite sides of the stiffener member, a larger number of integrated circuit chips may be put into the same sized volume previously used. The thermal conductivity of the mounting stiffener member permits such an arrangement.

It is clear that the use of this stiffener serving as heat sink in the center of the high-density package allows for three-dimensional cooling of the

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entire package. As is known, the printed circuit board material, FR4, provides an organic carrier.

While the integrated circuit chips have been described as utilizing a high thermal conductivity paste for mounting the bottom surfaces of the integrated circuit chips to the stiffener member, it is evident that other forms of mounting may be used which have good thermal conductivity and thermal dissipation characteristics.

While the present invention has been described with respect to preferred embodiments, numerous modifications, changes, and improvements will occur to those skilled in the art without departing from the spirit and scope of the invention.

| What | | | - × | |
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| wnai | 35 | CIRT | mea | 15. |

| 2 | 1. A high-density package for integrated circuit chips |
|---|--|
| 3 | comprising: |
| 4 | a thermally conductive member having a pair of opposite |
| 5 | sides, each of said sides having spaced areas adapted to have an |
| 6 | integrated circuit chip mounted thereon; |
| 7 | a plurality of integrated circuit chips, each having a top |
| 8 | and a bottom surface, one of said surfaces of each of said |
| 9 | plurality of chips being mounted respectively on one of said |
| 0 | areas of said thermally conductive member so that said plurality |
| 1 | of chips are mounted on said pair of opposite sides of said |
| 2 | thermally conductive member; and |
| 3 | a carrier member having a preselected electrically |
| 4 | conductive pattern thereon being electrically connected to the |
| 5 | other surface of each of said plurality of integrated circuit chips. |
| I | A package, as claimed in claim 1, wherein said carrier is |
| 2 | a flex carrier that is bent around said thermally conductive member to face said |
| 3 | other surfaces of said plurality of integrated circuit chips. |
| | |

| 1 | 3. A package, as claimed in claim 1, wherein said carrier is |
|---|---|
| 2 | a two-part printed circuit board facing said other surfaces, said two parts being |
| 3 | electrically connected to each other by an integral flexible cable. |
| 1 | 4. A package, as claimed in claim 1, wherein said integrated |
| 2 | circuit chips are mounted on said thermally conductive member by means of a |
| 3 | high thermal conductivity paste. |
| 1 | 5. A package, as claimed in claim 1, wherein said thermally |
| 2 | conductive member serves as a stiffener for said high-density package. |
| 1 | 6. A package, as claimed in claim 5, wherein said thermally |
| 2 | conductive member is made of aluminum. |
| I | 7. A package, as claimed in claim 5, wherein said thermally |
| 2 | conductive member is made of copper. |
| 1 | 8. A package, as claimed in claim 5, wherein said thermally |
| 2 | conductive member is made of Thermalgraph™. |

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| 9. A package, as claimed in claim 1, wherein said thermally |
|--|
| conductive member is formed with a plurality of open channels to permit the |
| passage of air or other fluids therethrough. |
| 10. A plurality of high-density packages for integrated circuit |
| chips, each of said packages being formed, as claimed in claim 1, and wherein |
| said packages are stacked one next to the other, with the carrier of each |
| package being electrically connected to the carrier adjacent thereto; and |
| a mother board electrically connected to one of said |
| carriers. |
| 11. A package, as claimed in claim 3, wherein said carrier is |
| an organic card made of FR4 material. |
| 12. A package, as claimed in claim 1, wherein said carrier is |
| connected to said other surface of each of said integrated circuit chips by solder |
| balls. |
| 13. A package as claimed in claim 3, wherein said carrier is |
| made of teflon |

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| 1 | 14. A package as claimed in claim 3, wherein said carrier is |
|---|--|
| 2 | made of ceramic. |
| 1 | 15. A package as claimed in claim 1, wherein said carrier is |
| 2 | connected to said other surface of each of said integrated circuit chips by wire |
| 3 | bonds. |

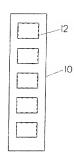


FIG. 1

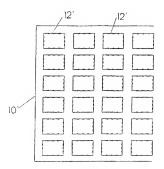


FIG. 2

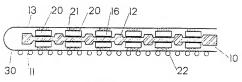


FIG. 3

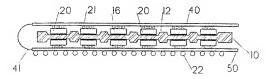
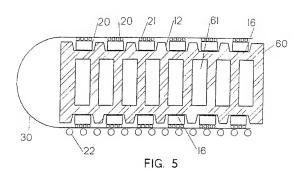
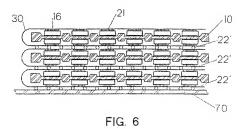


FIG.4





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C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|------------|--|-----------------------|
| х | "REMOVAL OF HEAT FROM DIRECT CHIP ATTACH CIRCUITRY" September 1989 , IBM TECHNICAL DISCLOSURE BULLETIN, VOL. 32, NR. 4A, PAGE(S) 346 - | 1,2,4,5, 10,12 |
| | 348 XP000039929 see the whole document | |
| Х | US 5 345 205 A (KORNRUMPF WILLIAM P) 6 September 1994 see column 9, line 46 - column 11, line 49; figures 1,2 | 1,2,4 |
| X | EP 0 629 000 A (ALCATEL NV ;ALCATEL ESPACE (FR)) 14 December 1994 see page 4, column 5, line 56 - page 5, column 7, line 30; figures 3,5,10 see page 6, column 9, line 31 - column 10, line 28 | 1,3-5, 10,14,15 |
| | | |
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| | | PC1/US 96/07290 | | |
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| C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT | | | | |
| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to daim No. | | |
| х | DE 43 29 936 A (AZDASHT GHASSEM ;LEUTENBAUER RUDOLF DIPL ING (DE)) 9 March 1995 see the whole document | 1,2,9, 10,12 | | |
| X | IBM TECHNICAL DISCLOSURE BULLETIN, vol. 30, no. 3, August 1987, NEW YORK US, pages 1353-1356, XP002024165 "CONCEPT FOR FORMING MULTILAYER STRUCTURES FOR ELECTRONIC PACKAGING" see the whole document | 1,2,5-7 | | |
| Х | US 5 050 039 A (EDFORS JOHN E) 17 September 1991 | 1,3,5,6, | | |
| A | see the whole document | 2,10 | | |
| A | see the whole document "DENSELY POPULATED, VERTICALLY STACKED MULTI CHIP MODULE" 1 April 1995, 1BM TECHNICAL DISCLOSURE BULLETIN, VOL. 38, NR. 4, PAGE(S) 59 - 62 XP000616073 see the whole document | 2,10 3,5,11 | | |
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...formation on patent family members

PCT/US 96/07290

| Patent document cited in search report | Publication date | Patent memi | | Publication date |
|---|---------------------|----------------|---|----------------------|
| US-A-5345205 | 06-09-94 | NONE | *************************************** | A |
| EP-A-0629000 | 14-12-94 | FR-A- CA-A- | 2706222 2125266 | 16-12-94 09-12-94 |
| DE-A-4329936 | 09-03-95 | NONE | | ********** |
| US-A-5050039 | 17-09-91 | NONE | | |